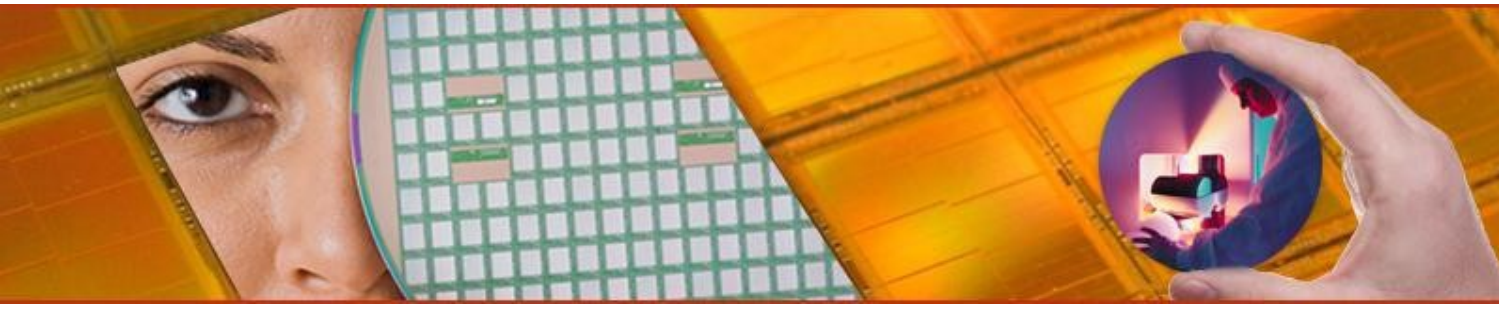
PowerLVS™

Accurate, Fast, and Easy-to-Use



KEY PRODUCT BENEFITS

- **Accuracy –** PowerLVS meets or exceeds foundry expectations
- **Shorter time to market -** LVS debugging from within familiar environments
- **Capacity –** PoweLVS was designed to easily handle the largest layouts

KEY PRODUCT FEATURES

- Ultra-fast scanning of layouts
- PWRL advanced rules & checks
- A suite of comparison algorithms
- Integrated LVS debugging
- Short Finder utility

Overview

PowerLVS is designed to complement PowerDRC and is driven by the same One-Shot scanning and the powerful yet easy-to-use rule language.

PowerLVS combines a fast, high-capacity extraction engine with a suite of comparison algorithms to deliver unmatched accuracy. PowerLVS offers ease of use in debugging and is integrated with popular layout and schematic viewers.

One-Shot Window Scan

One-Shot Window Scan is the proprietary scanning technology, an architectural quantum leap in LVS extraction that is the foundation of both PowerDRC and PowerLVS. The scanning captures multiple rules, layers, and operations at once and processes all of them simultaneously.

As technologies advance, the need for extraction to do more complex calculations and measurements increases significantly. POLYTEDA's physical verification technology based on One-Shot processing is essential to meet speed and capacity needs.

PWRL Advanced Rules & Checks

PWRL encapsulates advanced, complex rules into simpler syntax. The syntax encodes factors that are not considered at higher process nodes facilitating the implementation of advanced foundry rules.

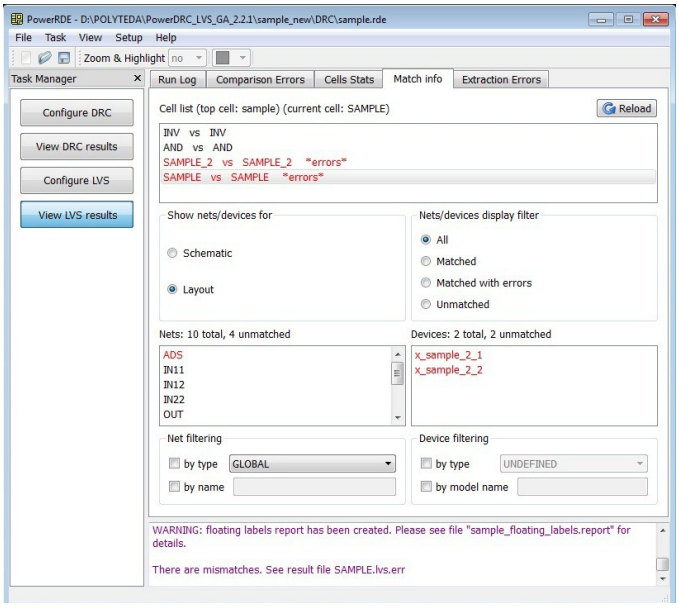


Figure 1. Top-level debug screen

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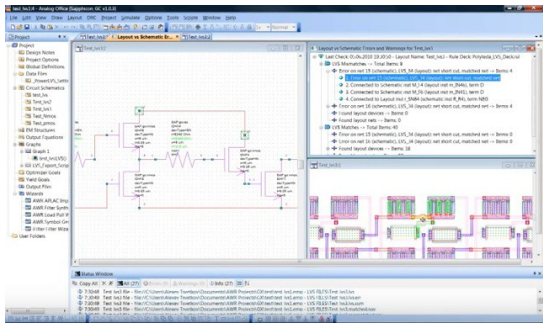

Figure 2. PowerLVS integrated with Analog Office

Comparison Algorithms

PowerLVS supports 7 effective comparison algorithms. They are applied automatically and dynamically depending on the type of blocks encountered within a design. As a design progresses through the comparison process, PowerLVS adapts and switches between algorithms "on-the-fly" to ensure accuracy at the highest level of performance.

Integrated LVS Debugging

The integrated debugging makes the tool extremely easy to use. It allows a user to select a net or device and probe it using the schematic or layout viewer integrated to their PowerLVS environment such as AWR Analog Office™, Cadence Virtuoso™, Synopsys Laker™, Symica, or KLayout. Fig.2 shows the integration with AWR Analog Office.

Special Features

- Hierarchical mode on demand
- Expanding of cell arrays
- Extraction errors reports with highlighting
- Extraction reports for multi-label nets, floating labels, open nets, malformed devices, hierarchical cells, etc.
- Netlist vs. netlist mode (NVN)
- Full support of blackbox operations

System Requirements

Supported operating system platforms:

- Linux 64 bit RedHat/CentOS 6+
- Windows 7 32/64 bit

Recommended hardware configuration:

- 2 GHz 64-bit (x64) processor
- 8 GB of system memory
- 16 GB of hard disk drive space

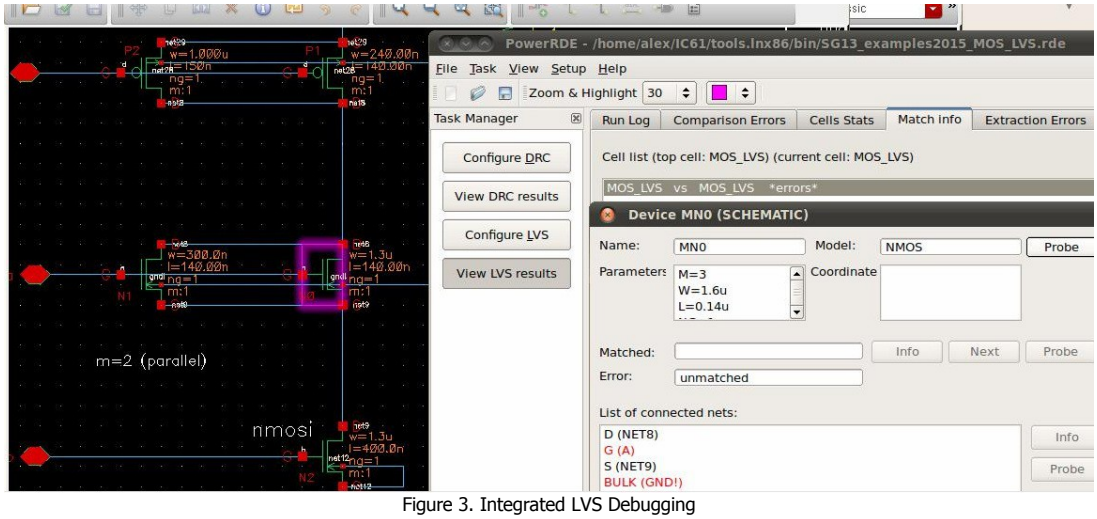

Figure 3. Integrated LVS Debugging

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