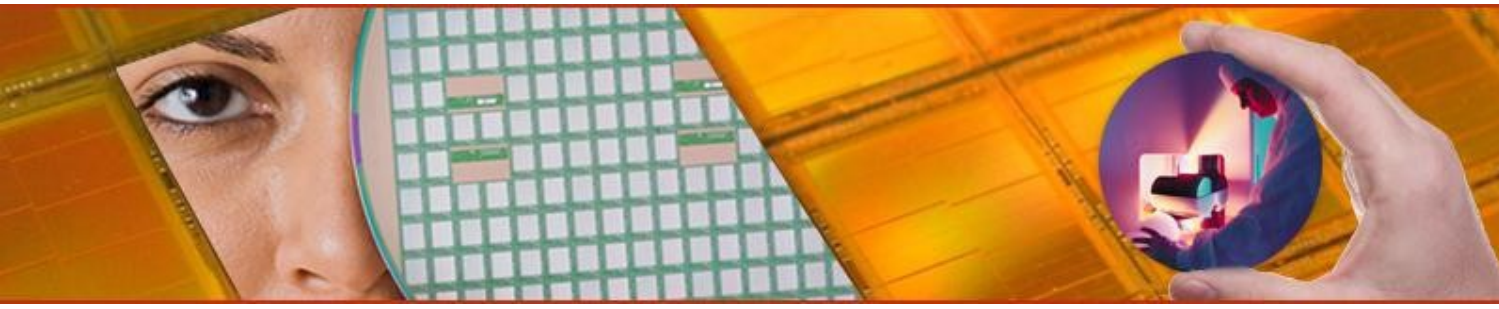
PowerDRC™
Fastest and Most Accurate Physical Verification



KEY PRODUCT BENEFITS

- Architected to address physical verification challenges for today's deep sub-wavelength nanometer process nodes—40nm and above
- Meets foundries accuracy requirements
- Delivers maximum per-CPU speed & capacity
- Predictable runtime, proportional to the number of devices
- Scalable capacity over single- & multi-CPU
- No need to "design around" the DRC tool to meet hierarchy considerations
- Extra level of IP protection that comes naturally with flat DRC

KEY PRODUCT FEATURES

- Ultra-fast scanning of layouts
- DRC, ERC, XOR, and fill layers generation
- Multi-CPU architecture, grid- and cloud-ready
- Easy-to-learn powerful rule language allowing fast and easy migration
- Easy-to-use GUI
- Readily integrates with popular design environments
- High flexibility due to a variety of run control parameters and pre-processing tools

One-Shot Window Scan

- A proprietary capability enabling simultaneous processing of multiple rules, layers, and operations
- Allows fast, and accurate physical verification at the most appropriate level of granularity across a variety of layout styles
- Extends perfectly into multi-CPU configurations
- Results in predictable runtimes proportional to the number of polygons to be processed

With shrinking geometries, the number of devices and hence the number of polygons per chip increase. With PowerDRC, the runtimes continue to be predictable (Figure 1).

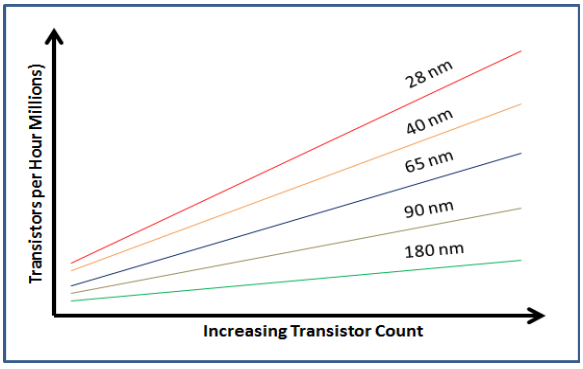


Figure 1. Linear & predictable runtimes

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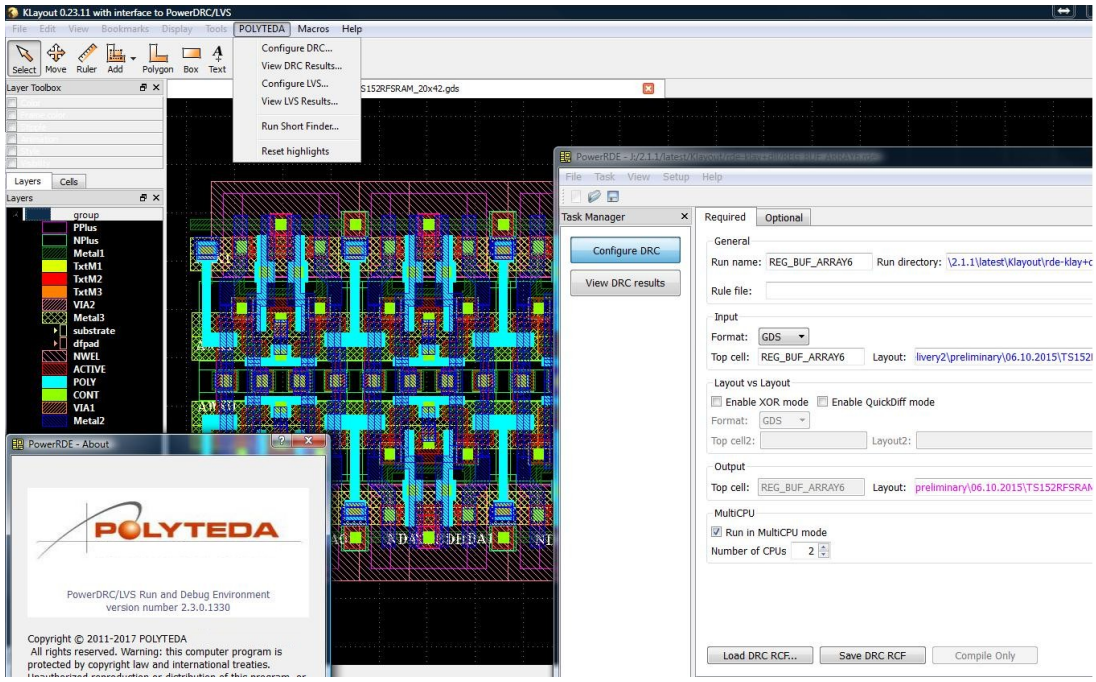

Multi-CPU Architecture

One-Shot Window Scan delivers the most powerful single-CPU DRC solution, and lends itself well for distributed processing over multiple CPUs without explosion of data. This improves DRC turnaround time and enables efficient and effective processing of large designs on a single host, in a grid, or in a cloud. Furthermore, the multi-CPU architecture leverages the performance benefits of one-shot scanning to maximize CPU efficiency per rule check.

PWRL design rule language

PWRL (pronounced Power-L) fits in with current rule deck architectures and flows allowing easy migration from existing PV systems. It also offers the ability to efficiently and effectively model the most complex rules and checks with fewer lines of code resulting in most comprehensive rule decks in terms of coverage with no fear of over- or under-checking. PWRL is really flexible due to its pre-processing capabilities like variables and conditionals.

Run and Debug Environment

POLYTEDA's PowerRDE provides the run and debug environment for PowerDRC with an easy-to-use GUI. It allows violation handling capabilities like assigning different status, grouping, filtering by area and location, sorting by number or status. With a layout viewer/editor integrated to PowerRDE, violations may be highlighted.

System Requirements

Supported operating system platforms:
- Linux 64 bit RedHat/CentOS 6+
- Windows 7 32/64 bit

Recommended hardware configuration:
- 2 GHz 64-bit (x64) quad-core processor
- 8 GB of system memory
- 16 GB of hard disk drive space

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