PowerDRC/LVS
Release Notes

Last update: May 2016
Product version: 2.2.1

New in this version

- Added hierarchical processing of cell arrays and standard cells to dramatically improve performance. The modes are switched on/off with new **ProcessStdCells** and **ProcessCellArrays** RCF parameters
- Added support of number and string variables in PWRL along with conditional directives **#if / #else**
- Added preprocessor directives **#define**, **#ifdef**, **#ifndef** for conditional rule compilation
- Added **$overunder** and **$underover** options to **$size**
- Added an example of using parameters extraction for the assessment of parasitic capacitances
- Added support of extraction by device nets. The mode is switched on/off with new **ExtractionByDeviceNets** RCF parameter
- Added a lot of minor improvements for integration with **Cadence Virtuoso**

Known issues

- Files in Laker format aren't supported by XOR mode
- During XOR operation, discrepancies of certain types on strip margins may be presented by two shapes in multi-CPU mode instead of one shape in single-CPU mode resulting in different total number of discrepancies reported in summary.
- There may be problems when processing large designs on 32-bit platforms, in particular:
  - XOR operation may run out of memory
  - Short Finder may run out of memory
  - Extraction may stop with a message about too many files open

  The issues do not manifest on 64-bit platforms.
- There may be a notable slowdown when processing big net lists with **MergeSplitGates** option switched ON. We recommend to turn the option off in such cases.
- Sometimes **PowerDRC/LVS** can be slowed down by anti-virus software installed on **Windows** machine. You may want to add an exception for run directory in your anti-virus software, so that files in the run directory are not checked for viruses.
- Sometimes when opening **DRC Results** window, **PowerRDE** loads results of the second to last run instead of latest results. Click **Reload** to update run results.
- In this version of **PowerDRC/LVS**, when working in the hierarchical mode of DRC/LVS in **Cadence Virtuoso**, user has to manually bring an active **Virtuoso** window to the front due to a known issue in **Cadence** API.

- When **PowerDRC/LVS** is running on **Windows** platform the number of characters in a path or a name that is specified as variable value in DRC RCF or NVN RCF cannot be greater than 255.

- Sometimes LVS operation may stop on comparison stage with message "PowerLVS has exited with code 111". If that is the case:
  - Please pay attention to case sensitivity, especially under Linux OS and check all settings
  - Double check your settings of **CaseIgnore** parameter
  - If you see different cell names for schematic and layout please use a bind file to specify corresponding pairs.

- In this version of **PowerDRC/LVS**, **PowerRDE** doesn't support definition of multiple layout files for Merge option of fill layers generation.